What is Claimed is:

1   1.   During the testing of the operation of a target
2 processing unit having a plurality of processors, a system
3 for synchronizing the trace streams from each of the
4 processors, the system comprising:
5   a plurality of processors, each processor including:
6   timing trace apparatus responsive to signals from
7 the processor unit, the timing trace apparatus generating a
8 timing trace stream; and
9   program counter trace apparatus responsive to
10 signals from the processing unit, the program counter trace
11 apparatus generating a program counter trace stream; and
12   synchronization apparatus applying sync signals
13 periodically to the timing trace apparatus and to the
14 program counter trace apparatus, the timing trace apparatus
15 including a sync marker in the timing trace stream in
16 response to the sync signal, the program counter trace
17 apparatus including a sync marker in response to the sync
18 signal;
19   wherein the program counter trace apparatus of each
20 processor is responsive to a global synchronization signal,
21 the program counter trace apparatus of each processor
22 generating global sync marker identifying the occurrence of
23 the global synchronization signal and relating the
24 occurrence of the global synchronization signal to the
25 timing trace stream.
26

1   2. The system as recited in claim 1 wherein the

2 global sync marker includes a global synchronization ID, a

3 program counter address, a timing index and a sync signal

4 ID.

5

6   3. The system as recited in claim 1 further

7 comprising:

8   data trace apparatus responsive to signals from the

9 processing unit, the data trace apparatus generating a data

10 trace stream, wherein the sync signals are applied to the

11 data trace apparatus, the data trace stream including a

12 sync marker in response to the sync signal.

13

14   4. The system as recited in claim 3 wherein a host

15 processing unit can relate the timing trace stream, the

16 program counter trace stream and the data trace stream of

17 all the processors.

18

19   5. The method for synchronizing the trace streams of

20 a plurality of processing units, the method comprising:

21   generating a timing trace stream, a program counter

22 trace stream, and data trace stream for each processing

23 unit;

24   including sync markers in the in the trace streams of

25 each processing unit permitting synchronization of the

26 trace streams of each processing; and

27   in response to a global synchronization marker applied

28 to each processing unit, including a global synchronization

1 marker in at least one trace stream of each processing
2 unit.

3

4   6.   The method as recited in claim 5 further
5 including:
6   in the global synchronization marker, including a
7 global synchronization ID, the global synchronization ID
8 identifying the global synchronization signal resulting in
9 the global synchronization marker.

10

11   7.   In a processing unit test environment wherein a
12 target processor includes a plurality of processing units,
13 each processing unit generating at least one trace stream,
14 a global synchronization marker for inclusion in at least
15 one trace stream for each processor, the marker comprising:
16   indicia identifying a global synchronization signal
17 applied to the processing unit issuing the trace stream;
18   indicia of the relationship of the occurrence of the
19 global synchronization signal to the clock of the
20 processing unit issuing the trace stream; and
21   indicia of the relationship of the occurrence of the
22 global synchronization signal to the processing unit
23 program execution.

24

25   8.   The marker as recited in claim 7 wherein the
26 indicia of the relationship of the global synchronization
27 signal to the processing unit program execution is a
28 program counter address of the processing unit.

1

2   9.   A system for testing the operation of a target

3   processing unit, the target processing unit including a

4   plurality of processing units, the system comprising:

5   a global signal synchronization generating unit;

6   each processing unit including;

7   a central processing unit; and

8   trace generating apparatus coupled to the central

9   processing, the trace generating apparatus generating a

10   least one trace stream;

11   wherein, the global signal generating unit applies a

12   global synchronization signal to the trace generating

13   apparatus of each processing unit, the global

14   synchronization signal resulting in a global

15   synchronization marker in at least one trace stream.

16

17   10. The system as recited in claim 9 wherein each

18   trace generating unit generates a plurality of trace

19   streams, each processing unit further including a periodic

20   sync signal, the periodic sync signal being applied to the

21   trace generating unit, the trace generating unit adding

22   indicia to the plurality trace streams permitting the

23   plurality of trace streams to be synchronized.

24

25   11. The system as recited in claim 9 wherein the

26   global synchronization marker includes a global

27   synchronization identification value and a value related to

28   the processing unit clock.

1

2   12. The system as recited in claim 9 further

3 comprising a host processing unit, the host processing unit

4 using the trace streams to reconstruct the operation of the

5 target processing unit.

6

7   13. The system as recited in claim 12 wherein the

8 global synchronization markers permit the operation of the

9 plurality of processors to be correlated.

10

11   14. The method of synchronizing the testing of a

12 plurality of processing units, each processing unit

13 including a trace generating unit for generating a

14 plurality of trace streams, the method comprising:

15   applying a global synchronization signal to the trace

16 generating unit of each processing unit;

17   generating in at least one trace stream of each

18 processing unit a global synchronization marker in response

19 to the global synchronization signal.

20

21   15. The method as recited in claim 14 wherein each

22 trace stream of a processor includes sync markers relating

23 the plurality of trace streams.